PVP 14

Code: EC6T1

III B.Tech - II Semester – Regular Examinations – May 2017

VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Explain briefly about Depletion mode transistor action.
b) What is Body effect?
c) What are stick diagrams?
d) Define Rise time.
e) Draw the circuit diagram of a two input AND gate using Pass transistor logic.
f) Write about limitations on scaling.
g) What is Full custom design?
h) What is FPGA?
i) What is Stuck-at model?
j) Compare CMOS and Bipolar transistor.
k) What is Programmable Logic Array?

PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Explain an nMOS fabrication process with suitable diagrams. 8 M

   b) Explain Latch up in CMOS circuits and how to avoid this problem? 8 M

3. a) What is meant by Sheet resistance R_S ? Explain the concept of R_S applied to MOS transistors. 8 M

   b) Realize the three-input NOR gate using CMOS technology. 8 M

4. a) What are the limitations of scaling VLSI circuits and explain them briefly. 8 M

   b) Realize a Logical function Y = AB + CD using transmission gates. 8 M

5. a) Design a Full Substractor using PLA. 8 M

   b) Explain about Gate Array Design. 8 M

6. a) Design Built-In-Self -Test (BIST) scheme for memories. 8 M

b) Explain the CMOS testing principles. 8 M